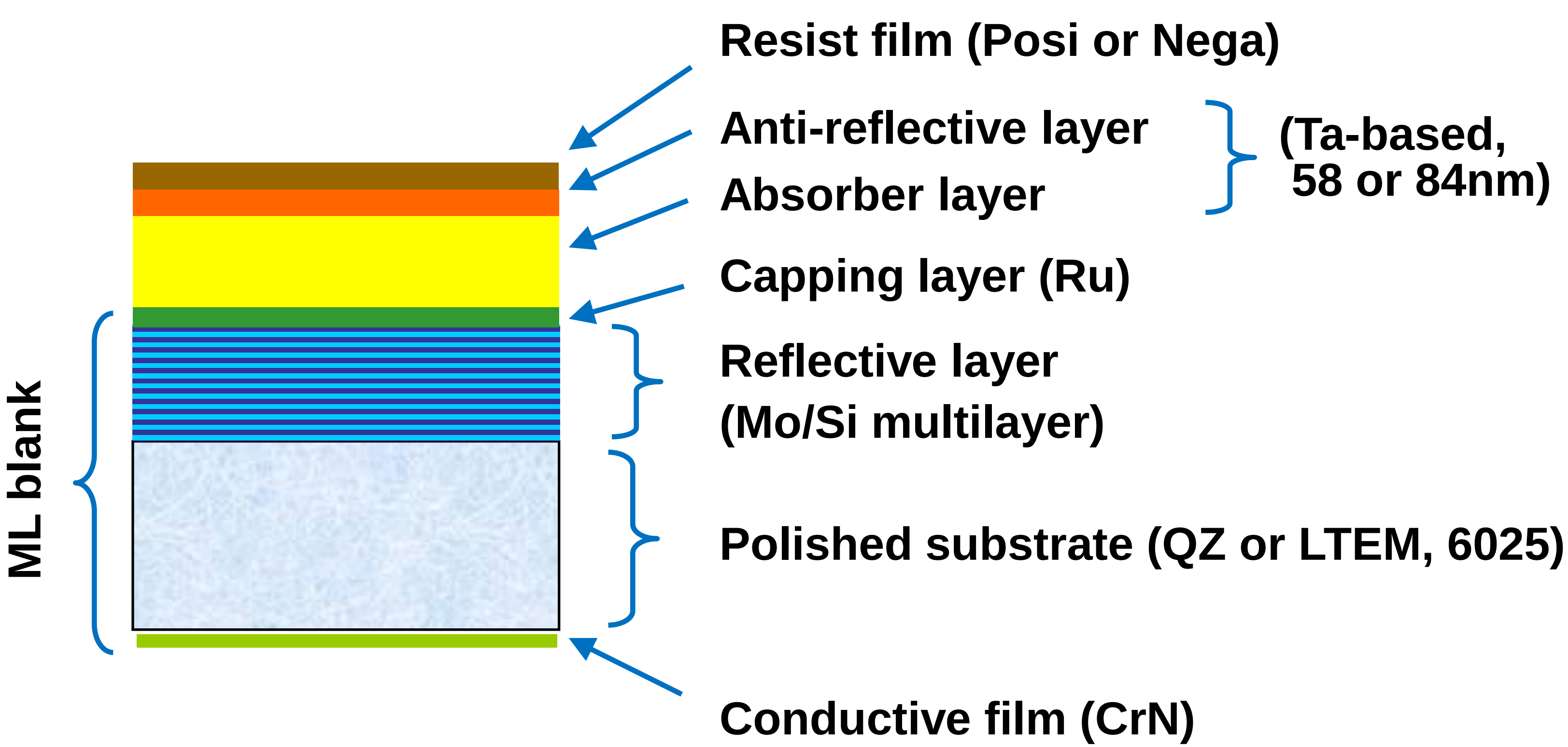
Development Status of EUVL Blank and Substrate

Asahi Glass Co. Ltd.
Hiroshi Nakanishi

Contents

1. Introduction

AGC EUVL blank structure



EUVL mask blank manufacturing process

- **AGC takes care of all essential materials and processes, *i.e.*, from LTEM material to film materials, from polishing process to cleaning process and to film coating process.**

Material synthesis	**Flame hydrolysis of Si and Ti source materials to form the Ti-doped SiO_2 glass ingot**
Slicing	**Slice the glass ingots into 6025 plates**
Lapping & Polishing	**Lap and polish to smooth & flat surfaces**
Cleaning	**Remove particles and polishing slurries**
Film deposition	**Deposit reflective, capping, absorber and ARC films**
Resist coat	

EUVL mask blank required properties

- **Here are the major properties required for the EUVL blank. AGC has in-house metrology toolset to evaluate all of these properties.**
- **AGC's current blank meets all requirements of the blank for the EUV PPT exposure tool, except for the defect and substrate flatness(<30nm).**

Material synthesis
↓
Slicing
↓
Lapping & Polishing
↓
Cleaning
↓
Film deposition
↓
Resist coat

Thermal expansion coefficient

Flatness, Roughness, Local slope, *Defect (Pit)*

Defect (Particle)

Surface & Embedded defect (particle)

EUV & DUV optical properties

Film stress (blank bow)

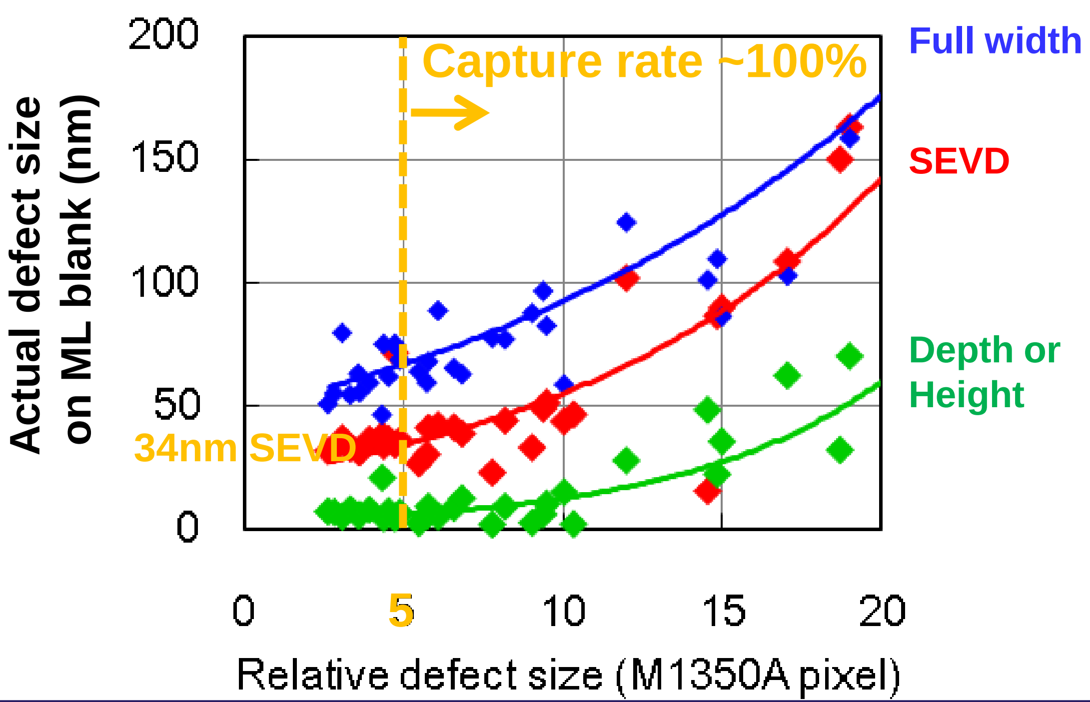
Durability to dry etch and wet cleaning chemicals

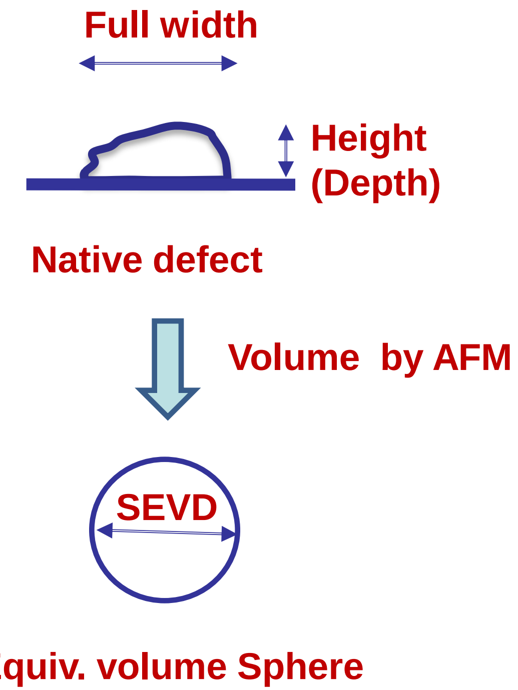
Dry Etch capability

2. Process development

Defect size definition

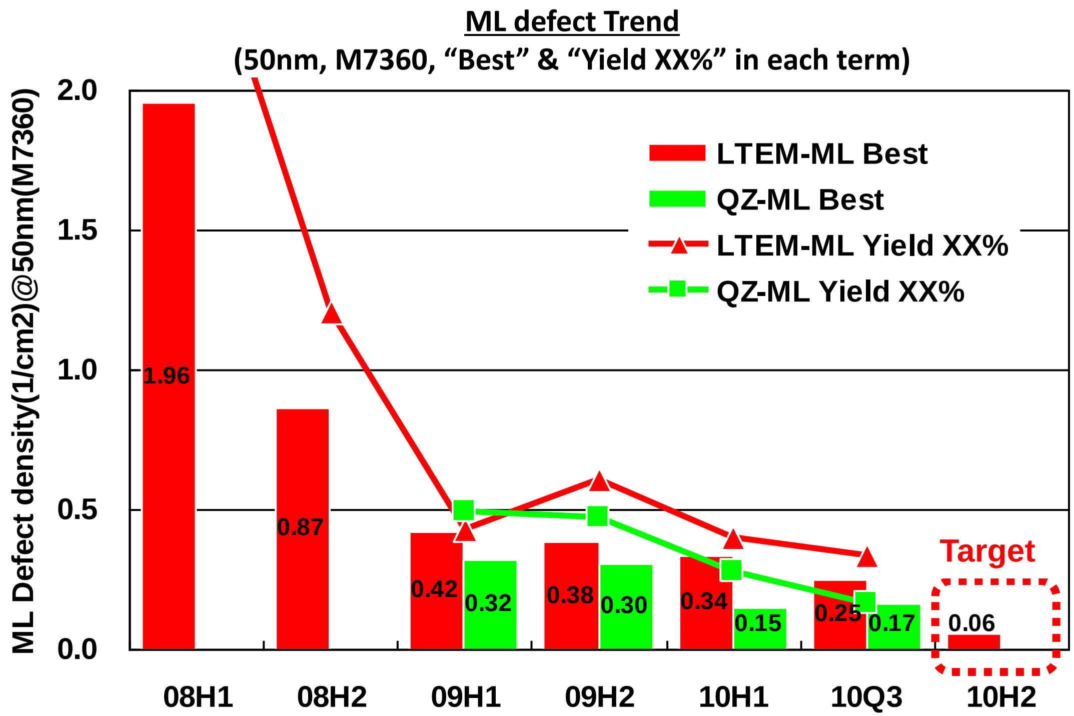
- The ML blank defect data was obtained by Lasertec M7360. The defect size was defined by the SiO2 sphere equivalent size.
- The other defect data were obtained by AGC in-house defect inspection tool (Lasertec M1350A). The defect size was defined by the sphere equivalent volume diameter (SEVD), which was obtained by measuring the native defect size with AFM. M1350A can capture defects as small as 34nm SEVD with ~100 % capture efficiency.

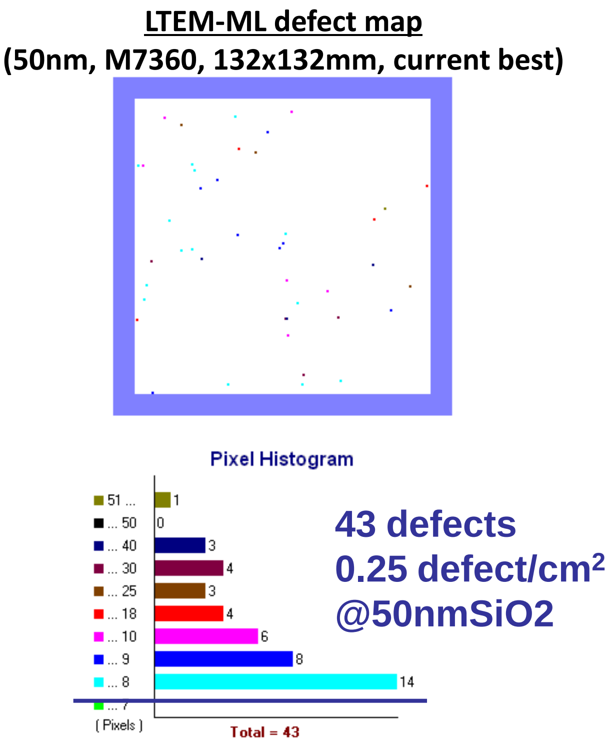




ML blank defect trend

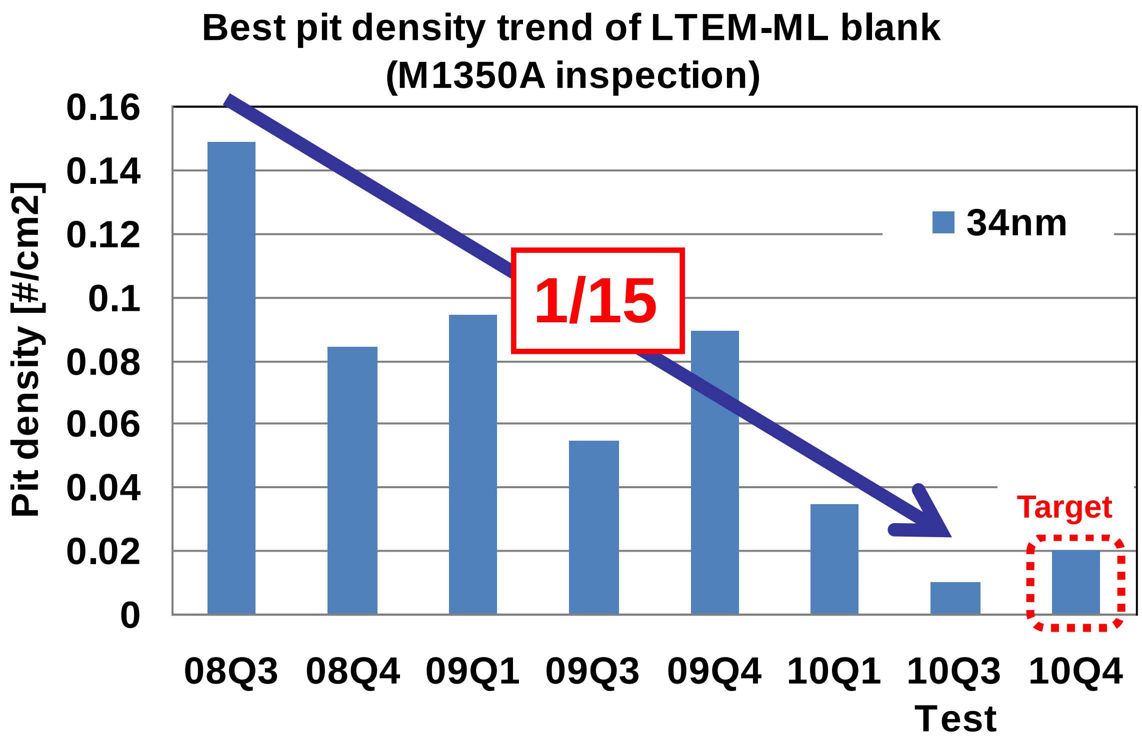
- The left figure shows the trend of the ML blank defect density inspected w/ Lasertec M7360. The substrate flatness was < 100~150nm in case of LTEM.
- Not only "Best" defect count but also "Yield XX%" defect count has been reduced continuously. The current "Best" defect density is LTEM-ML : 0.25/cm2, QZ-ML : 0.15/cm2 @50nm SiO2. The defect map shows the LTEM-ML best result. The majority of ML blank defect comes from substrate.





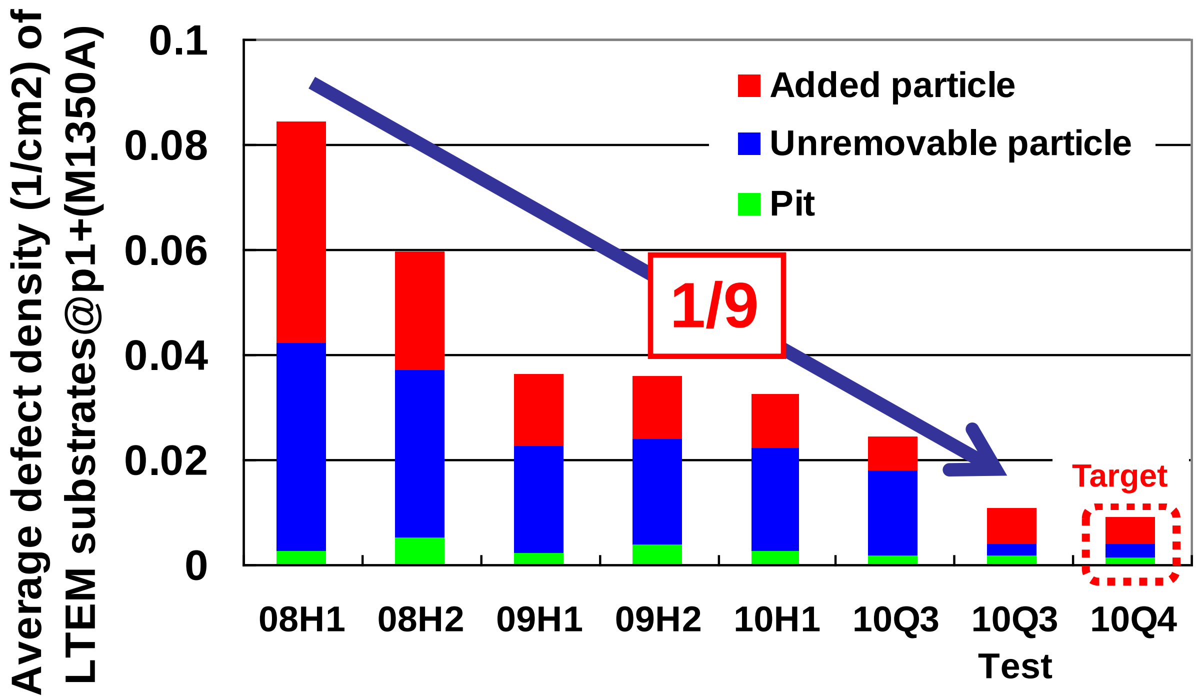
Substrate pit reduction

- This graph shows the best pit count trend of the LTEM-ML blank with <150nm substrate flatness.
- We have been continuously reducing the substrate pit by optimizing the polishing process parameters and the polishing materials.
- We recently demonstrated 2 pits LTEM substrate @34nm SEVD in 2010 Q3 test.



Substrate particle reduction

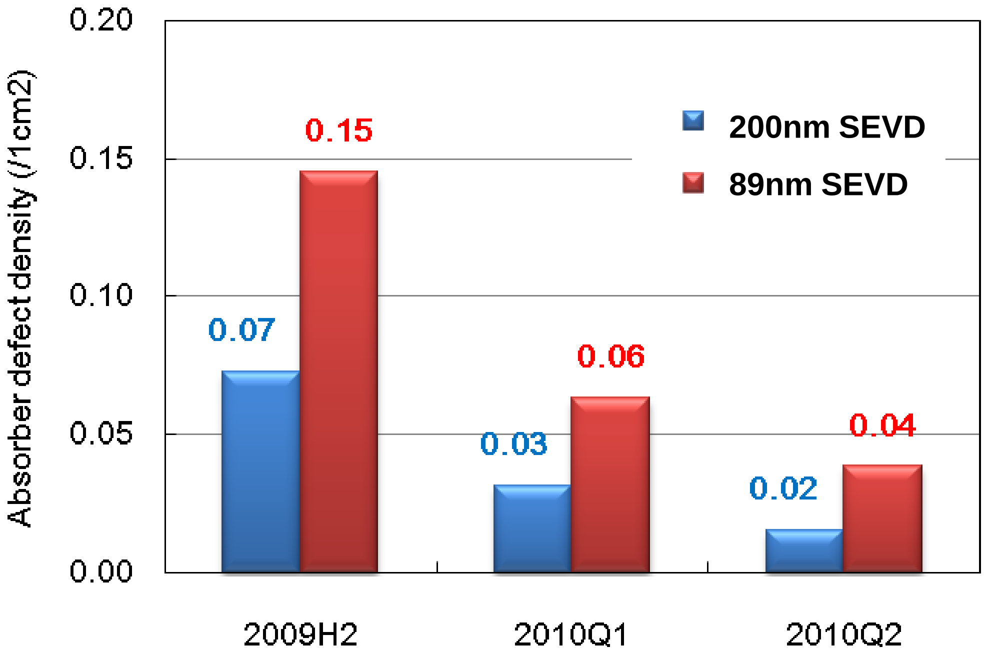
- The trend of the average defect count on LTEM substrates @ p1+ is shown below.
- To reduce un-removable particles, we implemented the new cleaning process. We have already achieved the 10Q4 target. Now we are further optimizing its cleaning process and material.
- We expect that "added particle" will be decreased further in 10Q4 by optimizing the final cleaning processes.



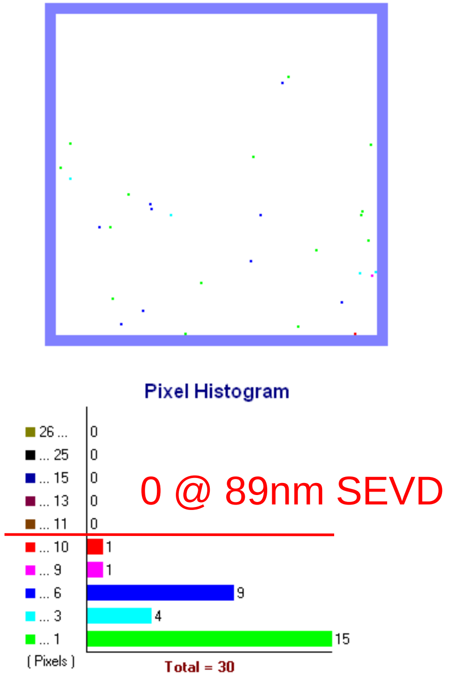
Absorber defect

- The left figure shows the trend of the average absorber defect.
- The current average absorber defect density is 0.02/cm2 (3defect/132x132mm) @ 200nm SEVD.
- The current best absorber defect density is 0 @ 89nm SEVD.

Absorber defect trend
(M1350A, Average)



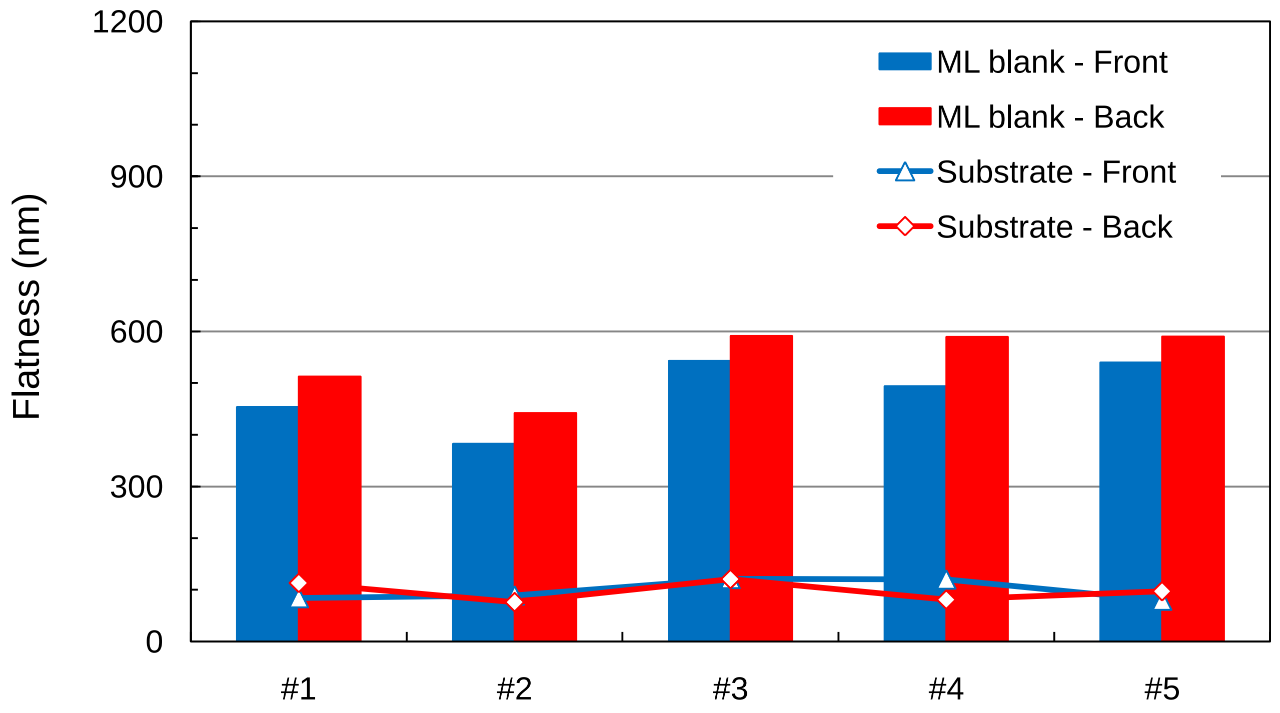
Absorber defect map
(M1350A, 142x142mm, Best)



2-2. Blank bow (ML blank flatness)

- **As results of the optimization of ML coating process parameters, we have already achieved <600nm blank bow, as shown in the below figure.**
- **AGC is currently investigating how to reduce the blank bow to <300nm.**

<u>Current blank bow</u>



3. Integrated performance of ML Blank

5. Integrated performance of LTEM-ML blank

Structure

CrN/LTEM/ML/Ru

CTE of LTEM

Mean CTE -2.1 ppb/K

CTE variation (PV) 3.9 ppb/K

Flatness (Front/Back)

Substrate 75/69 nm

Blank w/TaN&TaON <600/<600 nm

EUV Reflectivity

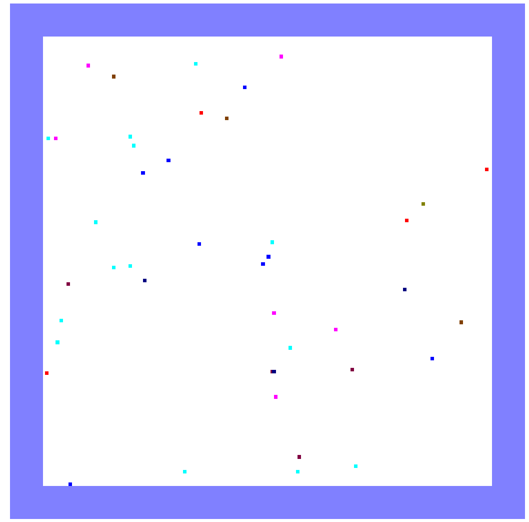
Peak %R 66.2 %

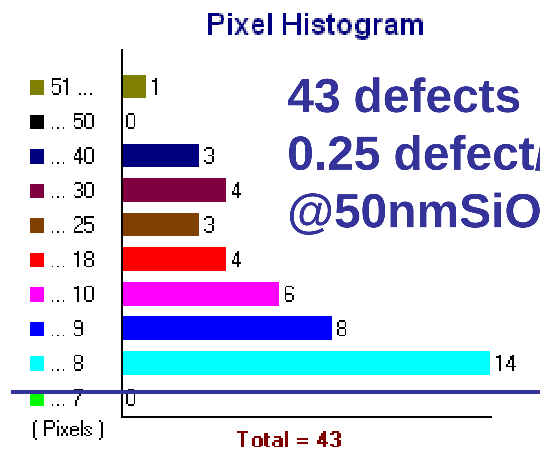
R range (Abs.) 0.2 %

Centroid λ (to target) 0.025 nm

λ range 0.021 nm

Defect map and histogram (M7360)





43 defects

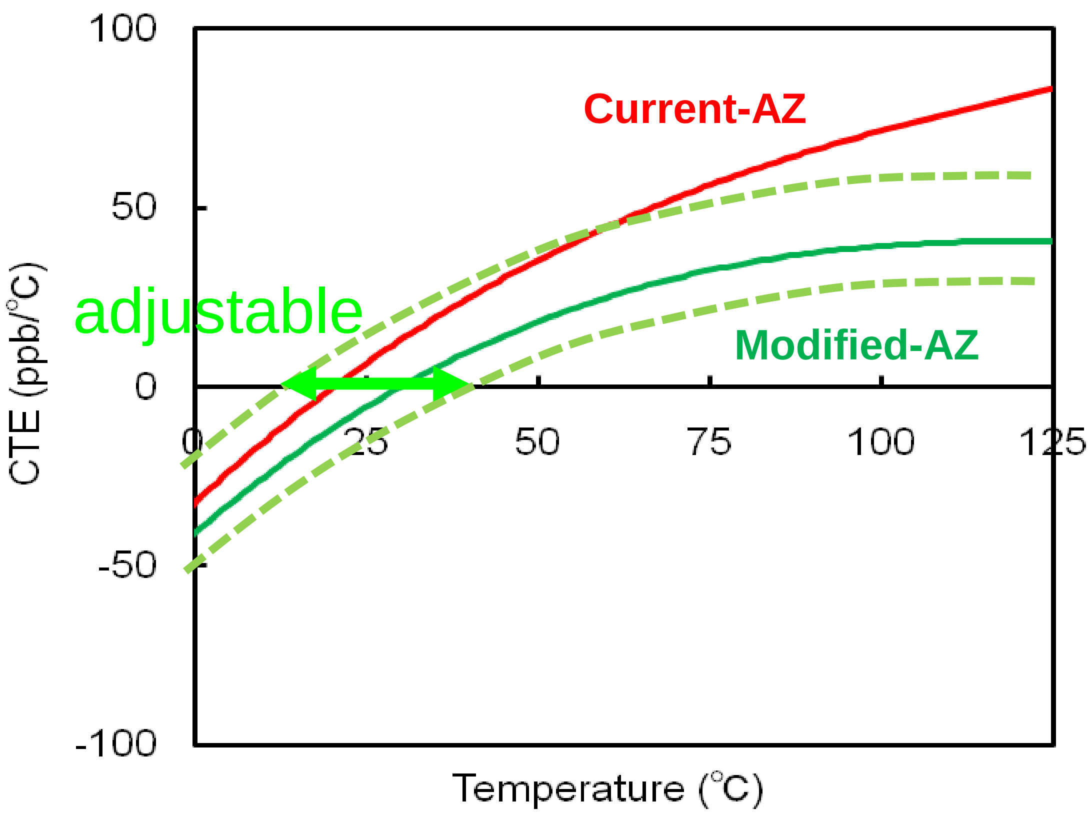
0.25 defect/cm^2

@50nmSiO2

4. Material development

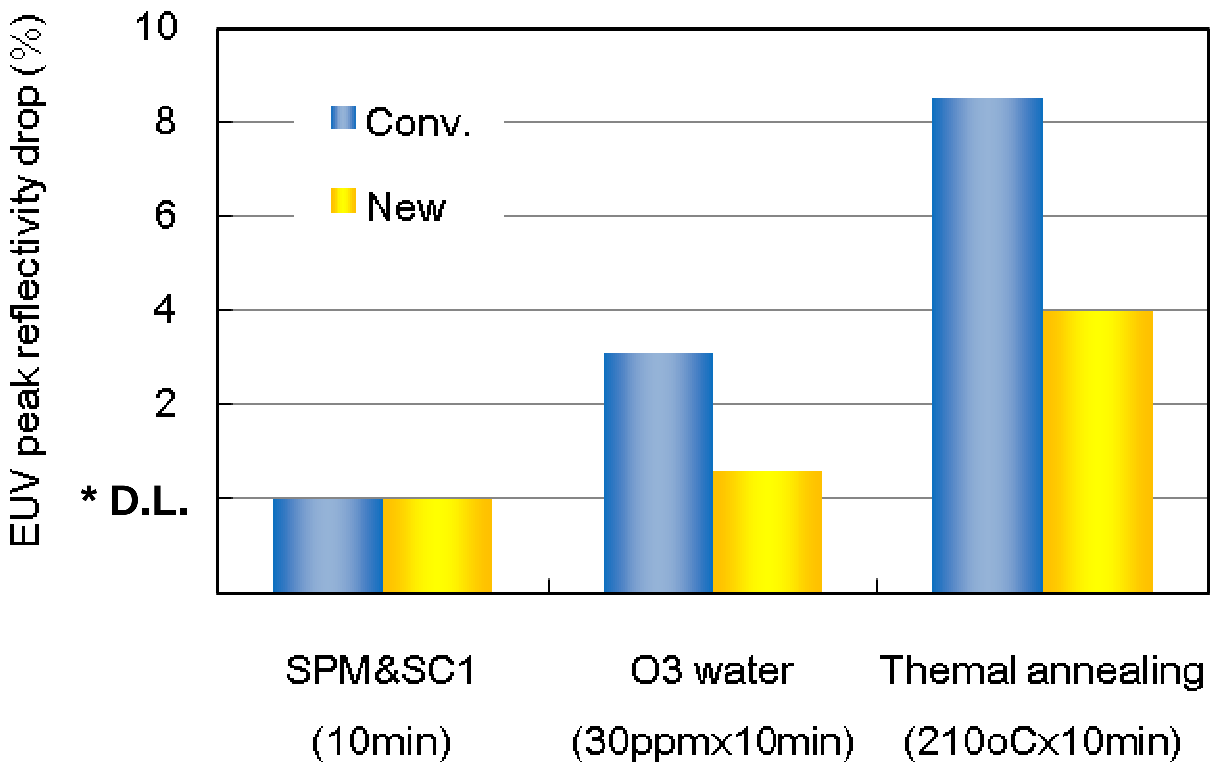
4-1. Modified substrate material (LTEM)

- **AGC has been developing the modified LTEM (AZ) which showed lower CTE slope than the current LTEM.**



4-2. New capping film

- **AGC has developed the new capping film which showed better durability to wet chemicals and thermal annealing.**



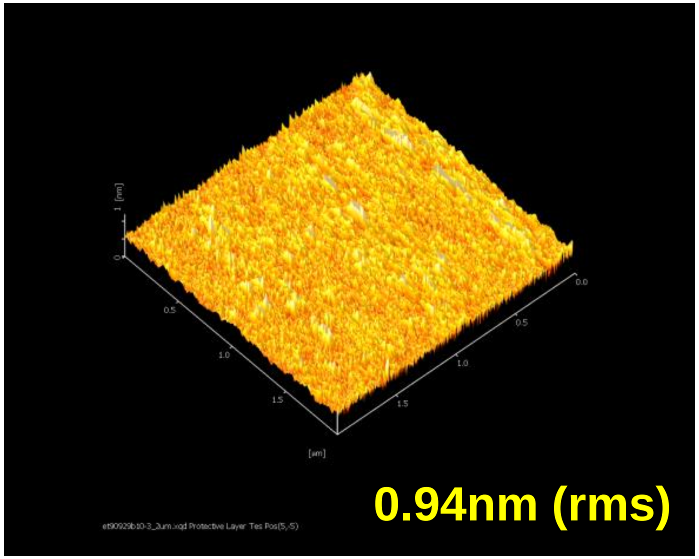
*** D.L. : Detection Limit**

4-2. New capping film

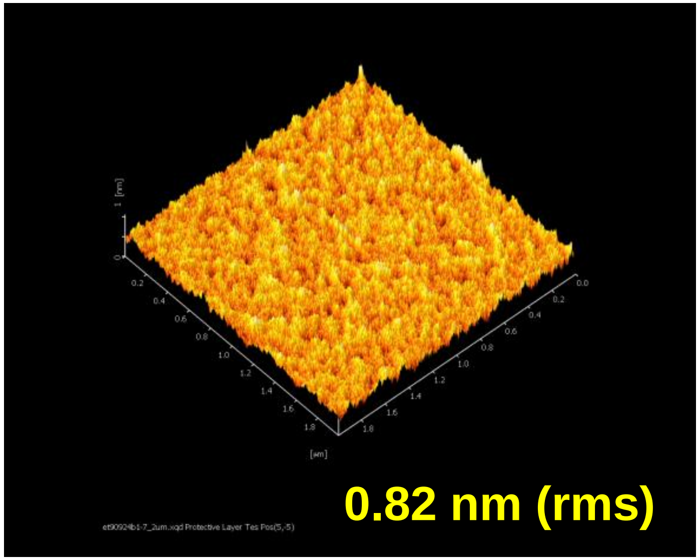
- **No increase in surface roughness upon O3-DI cleaning. It is another evidence of new capping film's good durability.**

<u>**Surface roughness of QZ/ML/Ru**</u>

Before O3-DI cleaning

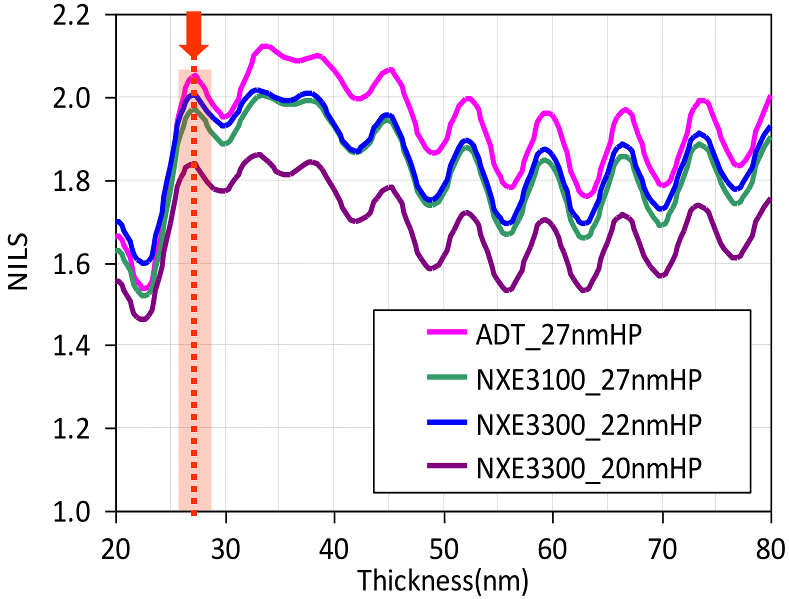


After O3-DI cleaning



4-3. Thin absorber material

- **AGC has been developing new materials suitable for thin absorber.**
- **AGC and IMEC have simulated the thickness dependency of NILS in candidate materials under various exposure tool settings and HPs, by using Synopsys Slitho-EUV and the EUV optical constants (n&k).**
- **We consequently found out the candidate material which could reduce its thickness to <30nm.**
- **AGC is currently optimizing the film deposition process of the candidate material.**



NILS v.s. Thickness of AGC' new material

Simulation condition

-Simulation tool : Synopsys Slitho-EUV

-Exposure setting : ADT, NXE3100, NXE3300

-HP: 27nm~20nm L&S

5. Summary and future plan

5. Summary and future plan

- AGC can provide 1st generation EUVL blanks suitable for EUVL pilot lines with PPT exposure tools.
- The only technical issue is the ML blank defect and its inspection toward the EUVL HVM.
  - AGC has been continuously reduced the defect by optimizing the blank fabrication processes, and the current best defect is 0.25/cm2 at 50nm SiO2 equivalent size.
  - Recently we could reduce the substrate defect drastically by optimizing the substrate polishing and cleaning processes. We are going to prepare LTEM-ML blanks in 2010/Q4 with these optimized substrate processes, and hopefully we will achieve <0.06/cm2 at 50nm in 2010/Q4.
- AGC is also developing 2nd generation blank including the material developments such as the modified LTEM, the new capping film material, and the thin absorber material. The 2nd generation blank will be suitable for 16nm hp and beyond.

	2010	2011	2012	2013	2014
1st generation	Process development		HVM		
2nd generation	Process & material development				HVM

Acknowledgement

- The author and AGC appreciate Dr. Andy Ma and Dr. Seh-Jin Park of Intel for their supports on the blank defect inspection with Lasertec M7360.

- The author and AGC appreciate Dr. Rik Jonckheere of IMEC for the lithography simulation of thin absorber.